31.3 A 4GS/s 4b Flash ADC in 0.18μm CMOS

Sunghyun Park[1], Yorgos Palaskas[2], Michael P. Flynn[1]

[1]University of Michigan, Ann Arbor, MI
[2]Intel, Hillsboro, OR

High-speed low-resolution ADCs are integral components of high-speed communication systems, such as serial links and UWB receivers. Flash ADCs generally achieve the highest sampling rates, with the comparator limiting maximum sampling speed. A flash ADC scheme, implemented in digital 0.18μm CMOS that achieves up to 4GS/s, with a low measured rate of metastability, is presented. High sampling speed is achieved without interleaving. High comparator speed is made possible through the use of inductors in the comparator core and the use of small fast devices. High measured SNDR (ENOB up to 3.97b), SFDR (-36.5dBc), and low DNL (< 0.15LSB) are achieved through a combination of DAC trimming and comparator redundancy.

Figure 31.3.1 shows the structure of the fully differential comparator. The comparator consists of a core, a cascade of two regenerative latching stages, and a DFF. The comparator core operates in *pre-amplification* and *latching* phases. The additional regeneration stages increase voltage gain, decreasing the risk of metastability. The latching stages [1] are identical, but are clocked on alternate phases.

The addition of a differential inductor in the comparator core (Fig. 31.3.1) not only improves the bandwidth of the preamplifier, but also reduces the regenerative time during latching ($M_{3\text{-}4}$, the load R, and L enabled). In a given CMOS technology, and for a given rate of metastability, sampling rate is limited by transistor f_t. Inductive loads are used to extend sampling rate, without increasing power consumption. The regenerative time constant can be considered by the effective resistance and capacitance

$$\tau(L) = \frac{C_{eff}}{g_{m3,4} - \frac{1}{R_{eff}}} \text{ with } C_{eff} = C - \frac{L}{R^2 + \omega^2 L^2}, \text{ and } R_{eff} = R + \frac{\omega^2 L^2}{R}$$

where C is the output capacitance, R is the output resistance, and ω is the signal frequency. Since $C_{eff} < C$ and $R_{eff} > R$, a reduced τ is achieved for all values of L. The inductor area is greatly reduced by using the parasitic resistance of the inductor as part of the load resistance. The inductors are implemented as stacked (the 3rd and 5th metal layers in series), differential inductors. Each 11.88nH inductor occupies 32μm by 32μm (10 turns, 0.4μm line width). The load resistance is comprised of the 203Ω parasitic resistance from the inductor (Q = 0.68 at 4GHz), and a 796Ω polysilicon resistor. With a 32μm separation between adjacent inductors, the magnetic coupling coefficient is less than 0.005 [2]. The cascode transistors, $M_{1\text{-}2}$, suppress kickback to the reference inputs.

Comparator offset is minimized with a combination of comparator redundancy and comparator DAC trimming. The use of redundancy significantly reduces the resolution and range required of the trim DAC to ensure high yield. For each code, there are two comparators, but only one is powered on and active in normal operation. Figure 31.3.2 shows the calibration scheme with a simplified comparator. A differential current DAC is connected to the output nodes of the preamplifier. During calibration, the inputs to the preamplifier are shorted. The calibration search begins by applying entire DAC current to one side of the preamplifier. The current is then steered in 1 DAC LSB increments until the output of the comparator changes. This scheme reduces not only the offset of the core, but also the input-referred offset of the following stages. If the search fails, then the redundant comparator is calibrated and used.

The trim current is provided by a thermometer-coded current DAC. The cascode transistors, $M_{1\text{-}2}$ (Fig. 31.3.2), reduce the capacitive loading on the preamplifier. Each current branch of the DAC consumes 4μA; this value is chosen to minimize the variance of the absolute value of the DNL of the ADC. The trimming DAC can correct comparator offsets up to ±0.64LSB to an accuracy of 0.08LSB. The calibration runs off a clock that is 1/256 of the ADC system sampling clock frequency, but during calibration the comparators sample at the full 4GHz rate. Measurement results show that calibration works reliably with 4GHz ADC system clock. The ADC automatically returns to normal operation when the calibration finishes. The total time for a calibration is 2.048μs with a 4GHz ADC sampling clock. The measured SNDR stays within 0.08 effective bits of its original value after 11 hours of continuous ADC operation at 3GS/s.

Fig. 31.3.3 shows the overall ADC. 15 comparators generate 15b thermometer code. A Wallace tree counter is used for thermometer-to-binary conversion, for increased immunity to metastability and sparkle codes. To ensure a proper operation of the counter at 4GS/s, the ADC uses two time-interleaved counters running at half of the comparator clock frequency (i.e. 2GHz). To facilitate testing of the prototype, the digital output from the encoder is decimated by 64. The clock buffer generates clocks for comparator ($Clk_{COMPARATOR}$), encoder ($Clk_{ENCODER}$,), and for DACs (Clk_{DAC}).

Fig. 31.3.4 is a die micrograph of the ADC. The device is fabricated in 0.18μm digital TSMC CMOS and packaged in a 52-pin LCC ceramic package. Each comparator set comprises of two comparators (for redundancy) with two differential inductors. Including the 30 inductors, the total active area (excluding the resistor ladder) is 0.88mm^2. The prototype runs off 1.8V analog and 2.1 to 2.5V digital supplies. (The higher digital supply compensates for a resistive voltage drop due to a layout error in the digital power routing.) Figure 31.3.5 shows the measured DNL and INL at 4GS/s (with 10MHz input). The DNL is between -0.14 and 0.15LSB, and the INL is between -0.20 and 0.24LSB after calibration. Figure 31.3.6 (a) shows SNDR versus clock frequency (f_S) with 100MHz input (f_{IN}). Measured ENOB is more than 3.89 effective bits (10MHz input) at 4GS/s after calibration. Figure 31.3.6 (b) shows the variation of SNDR versus f_{IN} with three different sampling frequencies after calibration. Jitter noise and package/pad loss dominate above f_{IN} = 0.9GHz. The ADC achieves an SFDR of -36.5dBc with f_{IN} = 0.3GHz and f_S = 2.6GHz, and -30.0dBc with f_{IN} = 0.7GHz and f_S = 3.4GHz. Using the method described in [3], no metastability error is detected in 10^{11} samples, indicating a BER less than 10^{-11}. The measured ENOB (f_{IN} = 0.3GHz, f_S = 2.4GHz) from the 4 ADCs evaluated is between 3.75 and 3.91. Figure 31.3.7 summarizes the ADC performance and the power consumption with various f_S. The analog circuitry (comparator core, regenerative stages, and resistor ladder) consumes 89mW at 4GS/s. Digital power consumption is proportional to f_S.

Acknowledgements:
The authors acknowledge the assistance of Ivan Bogue, JunYoung Park, Brendan Casey, and Stacy Ho. This work is supported by Intel.

References:
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[2] W.B. Kuhn, et al., "A 200 MHz CMOS Q-enhanced LC Bandpass Filter," *IEEE J. Solid-State Circuits*, vol. 31, no .8, pp. 1112-1122, Aug., 1996.
[3] A.G.W. Venes, et al., "An 80-MHz, 80-mW, 8-b CMOS Folding A/D Converter with Distributed Track-and-Hold Preprocessing," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1846-1853, Dec., 1996.

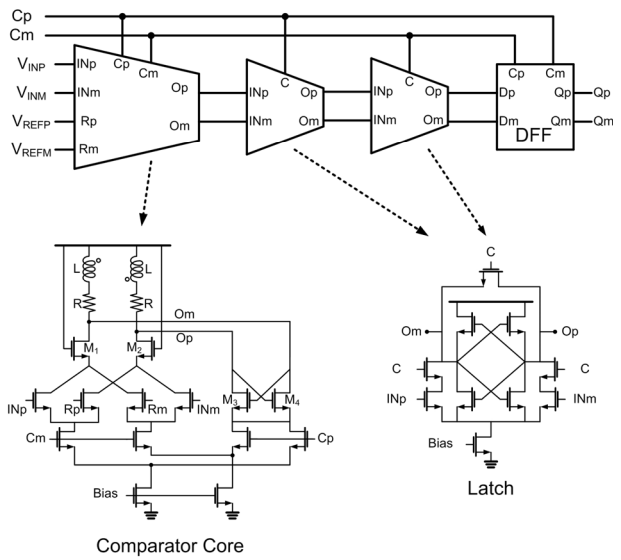

Figure 31.3.1: Comparator structure.

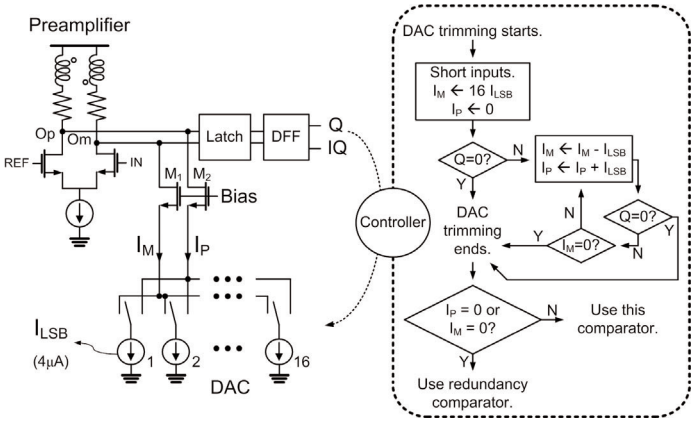

Figure 31.3.2: DAC trimming of simplified comparator.

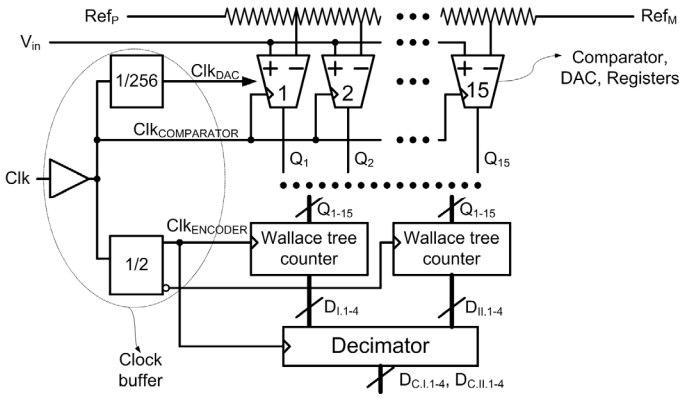

Figure 31.3.3: ADC structure.

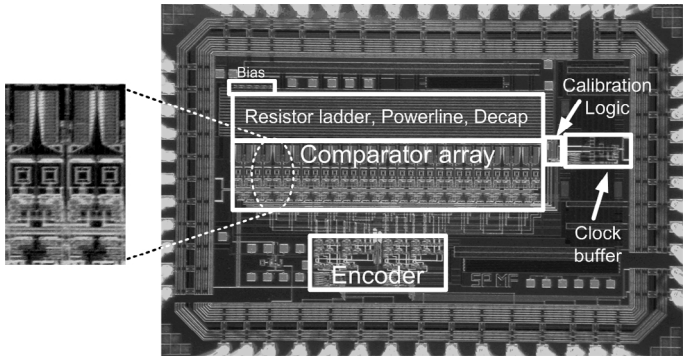

Figure 31.3.4: ADC die micrograph.

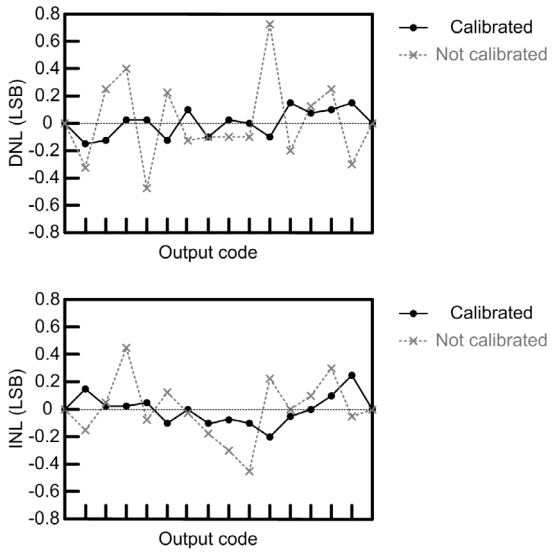

Figure 31.3.5: ADC linearity at 4GS/s.

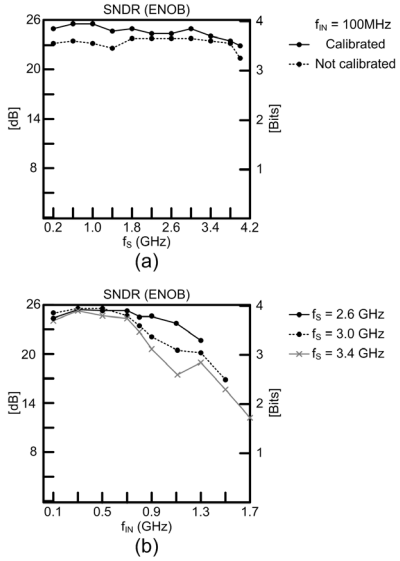

Figure 31.3.6: SNDR (ENOB).

Continued on Page 674

Technology	CMOS 0.18μm
Resolution	4 bits
Supply	1.8V (analog) 2.1-2.5V (digital)
Input range	0.46V_{PK} differential
Sampling rate	Max = 4GS/s Min < 100MS/s
Power	A: 89mW, D: 530mW @ f_S=4G, f_{IN}=0.1G
DNL, INL	DNL: -0.14 ~ 0.15 (LSB) INL: -0.24 ~ 0.20 (LSB) @ f_S=4G, f_{IN}=10M
ENOB	3.89 @ f_S=4.0G, f_{IN}=10M 3.48 @ f_S=4.0G, f_{IN}=0.1G 3.47 @ f_S=3.4G, f_{IN}=0.8G
BER	< 10^{-11} @ f_S=4G, f_{IN}=0.1G
Active area	0.88mm^2
Input cap	1.6pF
Package	LCC52

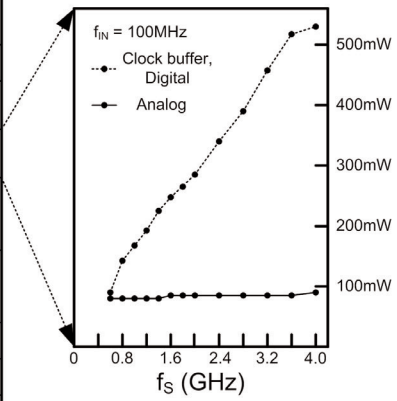

Figure 31.3.7: Performance summary.

